Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A delay cell, comprising:
a latch comprising a first circuit and a second circuit being cross-coupled together;
a first circuit logic gate and a first circuit capacitor both being electrically coupled to the first circuit such that the first circuit, the first circuit logic gate, and the first circuit capacitor being in series; and
a first input logic gate electrically coupled to an output of the first circuit, the first input logic gate is configured to switch states, and the first and second circuits are configured to switch states at time t1 in response to the first input logic gate switching states at time t2, with a delay time between t1 and t2 depending on the voltage level of a gate terminal of the first circuit logic gate.

[c2] 2. The delay cell of claim 1, further comprising a second circuit logic gate and a second circuit capacitor both electrically coupled to the second circuit such that the second circuit, the second circuit logic gate, and the second circuit capacitor being in series, wherein the delay time between t1 and t2 further depends on the voltage level of a gate terminal of the second circuit logic gate.

[c3] 3. The delay cell of claim 2, wherein the gate terminal of the first circuit logic gate and the gate terminal of the second circuit logic gate are electrically coupled together.

[c4] 4. The delay cell of claim 1, further comprising:
a first pull-up logic gate electrically coupled between the output of the first circuit and a voltage supply;
a first gate-terminal capacitor; and
a first gate-terminal logic gate,
wherein the first gate-terminal capacitor and the first gate-terminal logic gate are electrically coupled together such that the first gate-terminal capacitor and the first gate-terminal logic gate are in series between an input of the first circuit and a gate terminal of the first pull-up logic gate, and wherein the time delay between t1 and t2 further depends on the voltage level of a gate terminal of the first gate-terminal logic gate.

[c5] 5. The delay cell of claim 4, further comprising:
a second pull-up logic gate electrically coupled between the input of the first circuit and the voltage supply;
a second gate-terminal capacitor; and
a second gate-terminal logic gate,
wherein the second gate-terminal capacitor and the second gate-terminal logic gate are electrically coupled to-

gether such that the second gate-terminal capacitor and the second gate-terminal logic gate are in series between the output of the first circuit and a gate terminal of the second pull-up logic gate, and wherein the time delay between t1 and t2 further depends on the voltage level of a gate terminal of second gate-terminal logic gate.

[c6] 6. The delay cell of claim 5, wherein the gate terminal of the first gate-terminal logic gate and the gate terminal of the second gate-terminal logic gate are electrically coupled together.

[c7] 7. The delay cell of claim 1, further comprising a second input logic gate electrically coupled to an input of the first circuit, wherein the second input logic gate is configured to have states opposite to that of the first input logic gate.

[c8] 8. The delay cell of claim 1, further comprising:a cross-output logic gate; and
a cross-output capacitor,
wherein the cross-output logic gate and the cross-output capacitor are electrically coupled together such that the cross-output logic gate and the cross-output capacitor are in series between the output of the first circuit and an output of the second circuit, and wherein the

time delay between t1 and t2 further depends on the voltage level of a gate terminal of the cross-output logic gate.

[c9] 9. A method for operating a delay cell, the method comprising the steps of:
providing in the delay cell (i) a latch comprising a first circuit and a second circuit being cross coupled together, (ii) a first circuit logic gate and a first circuit capacitor both being electrically coupled to the first circuit such that the first circuit, the first circuit logic gate, and the first circuit capacitor being in series, and (iii) a first input logic gate electrically coupled to an output of the first circuit;
switching states of the first input logic gate; and
switching states of the first and second circuits at time t1 in response to the first input logic gate switching states at time t2, with a delay time between t1 and t2 depending on the voltage level of a gate terminal of the first circuit logic gate.

[c10] 10. The method of claim 9, further comprising the steps of:
providing further in the delay cell a second circuit logic gate and a second circuit capacitor both electrically coupled to the second circuit such that the second circuit, the second circuit logic gate, and the second circuit ca-

pacitor being in series; and

switching states of the first and second circuits in response to the first input logic gate switching states, with the delay time between t1 and t2 depending on the voltage level of a gate terminal of the second circuit logic gate.

[c11] 11. The method of claim 10, wherein the gate terminal of the first circuit logic gate and the gate terminal of the second circuit logic gate are electrically coupled together.

[c12] 12. The method of claim 9, further comprising the steps of:

providing further in the delay cell (i) a first pull-up logic gate electrically coupled between the output of the first circuit and the voltage supply, (ii) a first gate-terminal capacitor, and (iii) a first gate-terminal logic gate, wherein the first gate-terminal capacitor and the first gate-terminal logic gate being electrically coupled together such that the first gate-terminal capacitor and the first gate-terminal logic gate are in series between an input of the first circuit and a gate terminal of the first pull-up logic gate; and

switching states of the first and second circuits in response to the first input logic gate switching states, with the delay time between t1 and t2 depending on the volt-

age level of a gate terminal of the first gate-terminal logic gate.

[c13] 13. The method of claim 12, further comprising the steps of:
providing further in the delay cell (i) a second pull-up logic gate electrically coupled between the input of the first circuit and the voltage supply, (ii) a second gate-terminal capacitor, and (iii) a second gate-terminal logic gate, wherein the second gate-terminal capacitor and the second gate-terminal logic gate being electrically coupled together such that the second gate-terminal capacitor and the second gate-terminal logic gate are in series between the output of the first circuit and a gate terminal of the second pull-up logic gate; and
switching states of the first and second circuits in response to the first input logic gate switching states, with the delay time between t1 and t2 depending on the voltage level of a gate terminal of the second gate-terminal logic gate.

[c14] 14. The method of claim 13, wherein the gate terminal of the first gate-terminal logic gate and the gate terminal of the second gate-terminal logic gate are electrically coupled together.

[c15] 15. The method of claim 9, further comprising the steps

of:

providing in the delay cell a second input logic gate electrically coupled to an input of the first circuit; and

switching states of the second input logic gate in response to the first input logic gate switching states such that the states of the second input logic gate are opposite of that of the first input logic gate.

[c16] 16. The method of claim 9, further comprising the steps of:

providing further in the delay cell (i) a cross-output logic gate, and (ii) a cross-output capacitor, the cross-output logic gate and the cross-output capacitor being electrically coupled together such that the cross-output logic gate and the cross-output capacitor are in series between the output of the first circuit and an output of the second circuit; and

switching states of the first and second circuits in response to the first input logic gate switching states, with the delay time between t1 and t2 depending on the voltage level of a gate terminal of the cross-output logic gate.

[c17] 17. A structure, comprising:

a latch;

an input logic gate, electrically coupled to a first output of the latch; and

a first impedance circuit electrically coupled to the latch such that the first impedance circuit and the latch are in series, the first impedance circuit is configured to change its resistance in response to a control signal, and the latch is configured to switch states at time t1 in response to the input logic gate switching states at time t2, with a delay time between t1 and t2 depending on the resistance of the first impedance circuit.

[c18] 18. The structure of claim 17, wherein the first impedance circuit comprises a latch-coupled capacitor and a latch logic gate electrically coupled in series, wherein the resistance of the latch logic gate depends on the voltage level at a gate terminal of the latch logic gate.

[c19] 19. The structure of claim 17, further comprising:
a pull-up logic gate electrically coupled between the first output of the latch and a voltage supply; and
a second impedance circuit electrically coupled between a second output of the latch and a gate terminal of the pull-up logic gate,
wherein the delay time between t1 and t2 further depends on the resistance of the second impedance circuit.

[c20] 20. The structure of claim 19, wherein the second impedance circuit comprises a gate-terminal capacitor

and a gate-terminal logic gate electrically coupled in series, and wherein the resistance of the gate-terminal logic gate depends on the voltage level at a gate terminal of the gate-terminal logic gate.